

Figure 3. Copper etched off one side of laminate

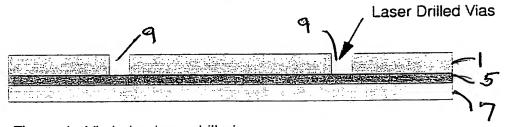
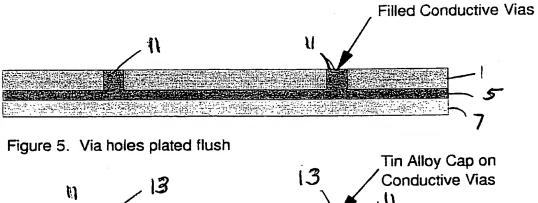


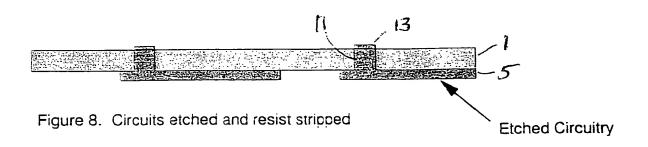
Figure 4. Via holes laser drilled



Conductive Vias

Figure 6. Filled vias overplated with solder alloy

7



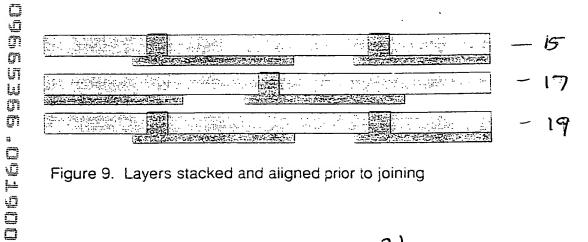


Figure 9. Layers stacked and aligned prior to joining

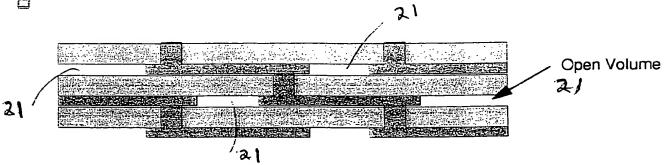


Figure 10. Circuits on adjacent layers joined by soldering

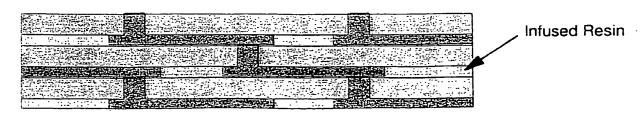


Figure 11. Resin infused and cured to fill and seal open areas

